Simulation of Single-Electron/CMOS Hybrid Circuits Using SPICE Macro-modeling

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The macro-modeling technique of single electron transistors has been applied to the SPICE simulation of single-electron/CMOS hybrid circuits. Several hybrid circuits such as an SET-NMOS pair and a single electron NOR-gate with CMOS buffers have been simulated and efficient interface characteristics have been demonstrated. This technique is simple to perform and does not require any modification of the SPICE internal source code.

I. INTRODUCTION

Recently, there has been great progress in the fabrication of various nano-devices utilizing silicon ULSI processing techniques [1]. Reliable room temperature operations have been demonstrated in a silicon single-electron quantum-dot transistor [2], a silicon self-assembled quantum-dot transistor [3], and various types of single-electron memory cells [4,5]. However, these single electron or quantum devices usually have extremely poor driving capabilities so that direct application to practical circuits is as yet almost impossible. One possible solution to overcome this problem is to build hybrid circuits consisting of single electron transistors (SETs) and CMOS interfaces [6] and in this case, simultaneous simulations of single electron circuits (SECs) and CMOS circuits are required for efficient circuit design and analysis. Usual SEC simulators such as MOSES [7], SIMON [8], KOSEC [9], and SENECA [10] are not compatible with SPICE and the only way of simultaneous simulation of hybrid circuit is to insert SEC simulation capabilities into SPICE source code. On the other hand, recently developed SPICE macro-modeling technique [9,11] is based on SPICE macro code and can be conveniently used for hybrid circuit simulation without having to modify the SPICE source code.

In this paper, the SPICE macro-modeling of SETs has been successfully applied to the simulation of single-electron/hybrid circuits. Several hybrid circuits such as an SET-NMOS pair and a single electron NOR-gate with CMOS buffers have been simulated and efficient interface characteristics are demonstrated.

II. REVIEW OF SPICE MACRO-MODELING OF SETS

Figure 1(a) shows the schematic diagram of an SET and its equivalent circuit. The macro-model representation of the equivalent circuit is summarized in Fig. 1(b) [11]. In Fig. 1(b), \( R_1, R_2, \) and \( R_3 \) is expressed with a cosine function to describe the Coulomb oscillation and \( D_2, D_3, V_p, \) and \(-V_p\) is expressed to describe the Coulomb staircase. The parameter values, \( CF_1 = 60, \) \( CV_p = 0.015, CI_2 = 0 \) \( \times 10^{-9}, CR_1 = 300 \) \( \times 10^6, \) and \( CR_2 = 100 \) \( \times 10^6, \) give the best fit of the current-voltage characteristics when \( C = 1.6 \) aF, \( C_g = 4.8 \) aF, \( R_t = 100 \) M\( \Omega, \) and \( T = 30 \) K. Figures 2(a) and (b) show the schematic diagram of the single electron NOR-gate and the complicated circuit consisting of three NOR-gates, respectively. Figures 3(a) and (b) shows the macro-model calculation results of two circuits shown in Fig. 2. The macro-model results (empty symbols) are in agreement with the Monte Carlo simulation results (filled symbols) [12] within 15 %, demonstrating the validity of the macro-model technique.

III. SIMULATION OF SE/CMOS HYBRID CIRCUITS

Figure 4 shows two typical examples of hybrid circuits. Figure 4(a) shows an inverter consisting of an SET with an NMOS load. The bias voltage \( (V_{dd}) \) is 0.015 V and the gate bias of the NMOS load \( (V_{gg}) \) is 0.5 V so that the NMOS load operates in the subthreshold region. The output of the inverter is connected to the 3-stage CMOS buffers. Figure 4(b) shows a hybrid circuit consisting of a single electron NOR-gate connected with 4-stage
Fig. 1. Macro-modeling of an SET (a) the equivalent circuit of an SET (b) the SPICE macro-model code ($C = 1.6$ aF, $C_g = 4.8$ aF, $R_t = 100$ MΩ, and $T = 30$ K).

CMOS buffers. The parameters of MOS transistors are notified in the figure where $W_n$, $W_p$, $L$, $t_{ox}$, $V_{TN}$, and $V_{TP}$ denote the NMOS channel width, the PMOS channel width, the channel length, the gate oxide thickness, the NMOS threshold voltage, and the PMOS threshold voltage, respectively. The channel widths of the first CMOS inverter are narrower than those of the others to reduce the load capacitance seen by the SEC. Multi-stage CMOS buffers are used for the amplification of

Fig. 2. Circuit diagrams for (a) a single electron NOR gate and (b) the complicated circuit consisting of three single electron NOR gates.

Fig. 3. The voltage transfer characteristics of SECs in Figs. 2(a) and (b). They are obtained from the SPICE macro-model. The filled symbols are Monte-Carlo results and the empty symbols are obtained from the SPICE macro-model.

Fig. 4. Schematic diagrams of hybrid circuits. (a) An inverter, consisting of an SET with an NMOS load, connected with 3-stage CMOS buffers. (b) A single electron NOR-gate connected with 4-stage CMOS buffers.
Simulation of Single-Electron/CMOS Hybrid Circuits Using SPICE Macro-modeling - Y. S. Yu et al.

Fig. 5. SPICE macro-model simulation results of the hybrid circuit shown in Fig. 4(a). (a) $I_{ds}$ of the SET and $V_{t}$ at the SET/NMOS node as a function of $V_{in}$. (b) Transient characteristics of $V_{t}$, $V_{i}$, and $V_{out}$ when the square pulse is applied to $V_{in}$.

The output signal ($V_{out}$) up to the full swing ($\pm 1$ V). However, the above CMOS buffer circuits consisting of CMOS inverters have some problem from a practical viewpoint because of the noise margin or MOS device parameter variation. In the future, we will be able to simulate hybrid circuits consisting of SEC circuits and new circuits such as the comparators over 10 bits with SPICE macro-model of SETs because the comparators over 10 bits can be designed independently enough to the noise margin or MOS device parameter variation.

**IV. CONCLUSIONS**

The macro-modeling technique of single electron transistors has been applied to the SPICE simulation of single-electron/CMOS hybrid circuits. Several hybrid circuits such as an SET-NMOS pair and a single electron NOR-gate with CMOS buffers have been simulated and efficient interface characteristics have been demonstrated. This technique is simple to perform and does not require any modification of the SPICE internal source code.

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